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Code No. : 14468 AS BO

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS), HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (E.C.E.) IV-Semester Advanced Suppl. Examinations, Aug./Sep.-2023

Computer Organization &amp; Architecture

Time: 3 hours

Max. Marks: 60

Note: Answer all questions from Part-A and any FIVE from Part-B

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	Evaluate the Sum of $1.011 \times 2^{-2}$ and $10.110 \times 2^{-1}$ ?	2	4	1	2
2.	Differentiate between Computer Organization and Architecture?	2	3	1	2
3.	Write any four Architectural features of 8085 $\mu$ p?	2	2	2	1
4.	List the address sequencing capability of micro program sequencer?	2	1	2	1
5.	Define Pipeline hazard? What are the various pipeline hazards?	2	2	3	2
6.	List any four characteristics of CISC core?	2	1	3	1
7.	Draw the diagram for source-initiated method I/O transfer using handshaking?	2	2	4	1
8.	Justify why DMA has priority over CPU when both require a Memory transfer at the same instant?	2	3	4	2
9.	Define page fault? List the most commonly used page replacement algorithms?	2	2	5	1
10.	Define Memory hierarchy? Draw the structure of memory hierarchy considered in computer systems?	2	2	5	2
<b>Part-B (5 × 8 = 40 Marks)</b>					
11. a)	Perform the Division using non-restoring division algorithm for the numbers (11) as dividend and (3) as divisor with suitable step wise evaluation?	4	3	1	2
b)	Explain the working of ripple carry adder with a suitable diagram?	4	2	1	1
12. a)	Write the broad classification of Instruction set of 8085 $\mu$ p? Write any five arithmetic instructions supported by 8085 $\mu$ p?	3	2	2	1
b)	Explain the working of Microprogrammed control unit with a suitable diagram?	5	2	2	2
13. a)	Define Amdahl's law? A non-pipelined system takes 50ns to process a task. The same task can be processed in a 6-Segment pipeline with a clock cycle of 10ns. Determine the speedup ratio of the pipeline for 100 tasks? What is the maximum speedup that can be achieved?	4	3	3	2
b)	Explain the working of Attached array Processor with a suitable diagram?	4	1	3	1

Contd... 2

14. a)	Explain the operation of Asynchronous serial transfer with a suitable diagram?	4	1	4	1
b)	Explain the operation of parallel priority interrupt method for I/O transfer?	4	1	4	1
15. a)	A computer system requires 2k bytes of RAM and 4K bytes of ROM. If each RAM chip size is 256X8 and ROM chip size is 1024x8?	4	3	5	2
	i) How many RAM and ROM chips are required?				
	ii) Draw the memory address map for the system?				
b)	Explain the concept of Associative memory with a suitable diagram?	4	2	5	1
16. a)	Write a short note on Computer Generations?	4	2	1	1
b)	Write a short note on stack organization of 8085 $\mu$ p?	4	3	2	1
17.	Answer any <i>two</i> of the following:				
a)	Explain the operation of Arithmetic pipeline with a suitable diagram?	4	2	3	2
b)	Explain the DMA type of data transfer in a computer system with a suitable diagram?	4	2	4	1
c)	Explain the Process of translation of virtual address to physical address with a suitable diagram?	4	3	5	2

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level - 1	20%
ii)	Blooms Taxonomy Level - 2	46.25%
iii)	Blooms Taxonomy Level - 3 & 4	33.75%

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